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Tiri Kris ; Verbaughede Ingrid ;

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

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Philip Brisk, Adam Kaplan, Ryan Kastner, Majid Sarrafzadeh

 October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**

 Full text available: [pdf\(203.26 KB\)](#)

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The increasing demand for complex and specialized embedded hardware must be met by processors which are optimized for performance, yet are also extremely flexible. In our work, we explore the tradeoff between flexibility and performance in the domain of reconfigurable processor design. Specifically, we seek to identify regularly occurring, computation-heavy patterns in an application or set of applications. These patterns become candidates for hard-logic implementation, potentially embedded in t ...

Keywords: control data-flow graph, hardware compiler, slack, template

2 [Architectures for cryptography and security applications: Efficient fingerprint-based user authentication for embedded systems](#)

Pallav Gupta, Srivaths Ravi, Anand Raghunathan, Niraj K. Jha

 June 2005 **Proceedings of the 42nd annual conference on Design automation**

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User authentication, which refers to the process of verifying the identity of a user, is becoming an important security requirement in various embedded systems. While conventional solutions for user authentication have relied on password-based mechanisms, they are increasingly being replaced by biometric technologies such as fingerprint, face, and voice recognition, which are known to provide higher levels of security for user authentication. This paper investigates the problem of supporting eff ...

Keywords: embedded systems, extensible processors, fingerprint, user authentication

3 [CAD: Power-efficient ASIC synthesis of cryptographic sboxes](#)

Guido Bertoni, Marco Macchetti, Luca Negri, Pasqualina Fragneto

 April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

 Full text available: [pdf\(140.35 KB\)](#)

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In this paper we present a novel methodology that can be used to design efficient hardware structures for a certain class of combinatorial functions. The methodology is primarily intended to achieve low-power synthesis of non-linear one-to-one functions on ASIC technology libraries and fits well for the synthesis of small cryptographic substitution box (Sbox) functional components; the latter are found in most secret key cryptographic algorithms, and usually represent their most relevant part in ...

Keywords: S-box implementation, cryptography, low power logic

4 JMTP: an architecture for exploiting concurrency in embedded Java applications with real-time considerations



Rachid Helaihel, Kunle Olukotun

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(139.94 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Using Java in embedded systems is plagued by problems of limited runtime performance and unpredictable runtime behavior. The Java Multi-Threaded Processor (JMTP) provides solutions to these problems. The JMTP architecture is a single chip containing an off-the-shelf general purpose processor core coupled with an array of Java Thread Processors (JTPs). Performance can be improved using this architecture by exploiting coarse-grained parallelism in the application. These performance im ...

5 Java bytecode compression for low-end embedded systems



Lars Ræder Clausen, Ulrik Pagh Schultz, Charles Consel, Gilles Muller

May 2000 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 22 Issue 3

Full text available: pdf(241.04 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

A program executing on a low-end embedded system, such as a smart-card, faces scarce memory resources and fixed execution time constraints. We demonstrate that factorization of common instruction sequences in Java bytecode allows the memory footprint to be reduced, on average, to 85% of its original size, with a minimal execution time penalty. While preserving Java compatibility, our solution requires only a few modifications which are straightforward to implement in any JVM used in a low-e ...

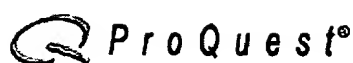
Keywords: Java bytecode, code compression, embedded systems

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B Ramakrishna Rau, Michael S Schlansker. Computer. New York: Apr 2001. Vol. 34, Iss. 4; p. 75

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The Press. Christchurch, New Zealand: Nov 21, 2000. p. 16

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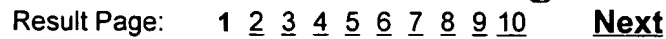
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